



# High Noise Floor Condition within the Prisma II 2:1 bdr Link Technical Bulletin

## Overview

### Introduction / Issue

Some customers have experienced an issue within the return path of systems using our 2:1 bdr equipment. The condition manifests itself as elevated noise across the entire return band.

An internal investigation concluded that the root cause resides in the receive processor. This condition can only occur during power up or power cycling of a node digital module. Even under these powering conditions the issue is a rare occurrence.

### Affected Units

Affected units are: PII-BDR-RP-2D (part number 738967)

**Note:** Internal testing has proved that this condition does not affect our 4:1 bdr equipment.

# Condition Clearing and Resolution

## Introduction

The condition relates to false synchronization of the receive processor at the initial data sequence and is caused by an FPGA firmware anomaly in the receive processor. Receive processors with FPGA code Revision G and earlier can exhibit this condition.

## Clearing the Condition

This condition can be cleared by performing any of the following:

- Removing and re-establishing the optical link
- Power cycling the receive processor
- Power cycling the node digital module

## Resolving the Condition

To permanently resolve this condition, update the FPGA code to Revision H. The FPGA code update can be performed at the Cisco factory at no charge under product warranty conditions.

## For Information

### If You Have Questions

If you have technical questions, call Cisco Services for assistance. Follow the menu options to speak with a service engineer.



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November 2012 Printed in USA

Part Number 4013649 Rev C