Configuring the Ring Limits on the PA-A3 and PA-A6 ATM Port Adapters

The PA-A3 and the PA-A6 ATM port adapters provide a way for you to limit the consumption of the receive ring and transmit ring resources on the NPE or NSE on a per-VC basis. The effect of these per-VC limits on the rings is a division of the resource into logical, per-VC queues. The default limits for both rings is calculated using internal logic based upon configured parameters (such as traffic shaping values) for the VC.

Chapter 2, "Cisco 7200 Series Architecture and Design for ATM Traffic Management," provides an in-depth discussion about how the receive ring and transmit ring structures work on the NPE or NSE in the overall processing of ATM traffic on the Cisco 7200 series router. It describes the relationship of the receive rings and transmit rings to the private interface pools on the NPE or NSE and also to the hardware buffers located on the ATM port adapters. It also discusses the relationship of the Layer 3 queues to the transmit ring.

This chapter describes how to optimize the ring limits on the PA-A3 and PA-A6 ATM port adapters. It includes the following sections:

Preparing to Configure the Ring Limits

Before you begin to configure the ring limits, you should have a good understanding of the Cisco 7200 series architecture and how the router processes ATM traffic.

Caution It is important to consider that the ring limits for the receive and transmit side are effectively operating against the same resource—particles within the private interface pool. Therefore, you must be very careful if you plan to tune these limits. Just as with adjustments to the buffer pools, improper settings for the receive ring or transmit ring limits can adversely impact system performance. In this case, adjustments to either side of the ring limits can impact the performance of both receiving and transmitting packets. Only modify the ring limits after careful evaluation of network impact or when recommended by technical support personnel.

Architecture Overview

This section reviews some of the important characteristics about the memory architecture during ATM processing that you should understand as you prepare to configure the ring limits. For more details, see Chapter 2, "Cisco 7200 Series Architecture and Design for ATM Traffic Management."

There are several memory structures that are used in the processing of ATM traffic on a Cisco 7200 series router. Some of these structures are located on the ATM port adapter hardware itself, while others are located on the NPE or NSE:

- Transmit and receive buffers—Particle-based hardware buffers located on the PA-A3 and PA-A6 ATM port adapters where actual content is stored upon receipt of ATM cells or in preparation of cell transmission. These buffers are fixed and you cannot optimize them. A DMA engine transfers content between the hardware buffers on the ATM port adapter and the private interface pool on the NPE or NSE.
- Private interface pool—Particle-based memory located on the NPE or NSE where actual packet content also is stored for receive and transmit processing. The private interface pool that is associated with the ingress interface (where the data is received from the network) stores the content. The private interface pool is typically a static pool that you cannot optimize. For the PA-A3 and PA-A6 ATM port adapters, the default number of particles in the private interface pool varies by the type of NPE or NSE in use. For more information, see Table 2-1 on page 2-7.
- Transmit and receive rings—Control structures located on the NPE or NSE that point to the stored location of packets in the private interface pool for receive or transmit processing. A corresponding receive ring and a transmit ring control structure is associated with each physical interface on the Cisco 7200 series router.

  You can optimize the size of the receive and transmit rings on a per-VC basis, which effectively determines how much of the private interface pool can be used for receive and transmit processing over that VC.

Ring Limit Overview

Operation of the receive rings and transmit rings is described in detail in the "Receive Rings and Transmit Rings" section on page 2-10. This section provides an overview of some of the important concepts about the ring limits for PA-A3 and PA-A6 ATM port adapters:

- There is a single receive ring and a single transmit ring corresponding to any physical interface on the Cisco 7200 series router.
- For the ATM port adapters, each entry in the receive ring or transmit ring shares a one-to-one correspondence with a particle stored in the private interface pool for a packet.
- The ring limit creates a logical division of a ring's total resource into per-VC queues. In other words, when an ATM port adapter supports traffic from multiple VCs, the ring limit places a boundary on the number of private interface particles that can be used by that VC.
- The implementation of ring limits affects the number of particles available in the private interface pool to store data for a given VC. You can interpret the ring limit as a threshold for particle usage by a VC.
- You specify the receive ring limit as a percentage of the private interface pool, and the transmit ring limit as a number of ring entries. Each of these limits translates to a number of particles in the private interface pool. It is important to recognize that although there are two different limits whose functions are based on whether you are in the receive stage or transmit stage of processing, both the receive ring limit and the transmit ring limit affect the same resource—particles in the private interface pool of the ingress interface.

Configuring the Receive Ring Limit

This section provides guidelines for configuring and verifying the receive ring limit. It includes the following topics:

Receive Ring Limit Configuration Guidelines

Use the following guidelines when planning to tune the receive ring limit:

Caution It is important to consider that the ring limits for the receive and transmit side are effectively operating against the same resource—particles within the private interface pool. Therefore, you must be very careful if you plan to tune these limits. Just as with adjustments to the buffer pools, improper settings for the receive ring or transmit ring limits can adversely impact system performance. In this case, adjustments to either side of the ring limits can impact the performance of both receiving and transmitting packets. Only modify the ring limits after careful evaluation of network impact or when recommended by technical support personnel.

- Consider tuning the per-VC receive ring in the case where a higher throughput ingress ATM interface might be feeding several slower egress serial interfaces.

  Private interface particles are not freed until the packet contents are transferred to the outbound port adapter or they are transmitted. This means that slow egress interfaces can tie up particle resource in the private interface pool, making the number of particles to receive data limited or unavailable for the receive ring. To help minimize this condition, you can increase the value of the **rx-limit** command.
- An indication that a VC is exceeding its receive ring limit is an increase in the number of ignored errors on the ATM interface, or input drops on the VC. For more information, see the "Monitoring Ring Limits and Resource Usage" section on page 7-12.
- Configure the **rx-limit** command as a percentage of the total particles in the private interface pool. Not all VCs need to add up to 100 percent. For example, it is possible to allow every VC to use up to 50 percent of the available resource. In this case, no more than two VCs would be able to use the full 50 percent at any given time or resource would not be available.
- You can configure the receive ring limit for a VC to be 100 percent, or the entire particle pool.

Default Values for the Receive Ring Limit

The default value for the receive ring limit is calculated internally based on the traffic shaping configuration on the VC using the following logic:

If PCR > 200

A = Min (PCR/200, Rx-Threshold)

Else

A = 0

Rx-Limit = Max (A, (MTU/particle_size) x 2)

The following further describes some of the variables used in this logic:

- The ATM port adapter sets the Rx-Threshold as the maximum Rx-limit that any VC on a given ATM interface can have. The Rx-Threshold is determined as 2/3 of the total number of available particles in the private interface pool for that ATM interface. For example, if the private interface buffer is 1200 particles, then the Rx-Threshold is 2/3 x 1200, which is 900. You can view the Rx-Threshold value using the **show controllers atm** command.

Note The Rx-Threshold is used only for computing the default receive ring limit. You can manually configure the **rx-limit** command on a VC to be 100 percent of the particle pool.

- The default maximum transmission unit (MTU) on the PA-A3 and PA-A6 ATM port adapters is 4470 bytes.

  The MTU defines the largest size of packets that an interface can transmit without needing to fragment. IP packets larger than the MTU must go through IP fragmentation procedures. Most Cisco ATM router interfaces use a default MTU size of 4470 bytes. This number was chosen to match Fiber Distributed Data Interface (FDDI) and High-Speed Serial Interface (HSSI) interfaces for autonomous switching. Cisco ATM router interfaces support an MTU between 64 and 17966 bytes. You can use the **mtu** interface configuration command to modify the default value.
- The particle_size value is 512 bytes, which is the size of the private interface pool particles.

Receive Ring Limit Configuration Example

Caution The **rx-limit** ATM VC configuration command is an internal command. Therefore, you must run the **service internal** global configuration command to access the **rx-limit** ATM VC configuration command. Any commands revealed by the use of the **service internal** command are unsupported.

The following example specifies that PVC 1/100 can use 25% of the private interface particle pool when receiving traffic:

```
Router# configure terminal
Enter configuration commands, one per line.  End with CNTL/Z.
Router(config)# service internal
Router(config)# int atm 1/0.1
Router(config-subif)# pvc 1/100
Router(config-if-atm-vc)# rx-limit 25
Router(config-if-atm-vc)# end
```

Verifying the Receive Ring Limit and Particle Buffers

To verify the number of particles in the PA-A3 or PA-A6 private interface pool and how much of the pool is available to a particular PVC for receive processing, complete the following steps:

Step 1 To view the total number of particles in the PA-A3 or PA-A6 private interface pool, which are allocated when data is received on that interface, use the **show controllers atm** command and observe the "rx buffers" field. In this example, there are 1200 total particles of size 512 bytes available in the ATM private interface pool:

```
Router# show controllers atm 5/0
Interface ATM5/0 is up
Hardware is ENHANCED ATM PA - OC3 (155000Kbps)
Framer is PMC PM5346 S/UNI-155-LITE, SAR is LSI ATMIZER II
Firmware rev: G127, Framer rev: 0, ATMIZER II rev: 3
  idb=0x62948598, ds=0x6294FEA0, vc=0x6297F940
  slot 5, unit 2, subunit 0, fci_type 0x0056, ticks 120012
  1200 rx buffers: size=512, encap=64, trailer=28, magic=4
[text omitted]
```

Step 2 To monitor how much of the private interface pool is currently allocated, use the **show buffers** command. The following example shows that all 1200 particles are in use (shown as "1200 hits") and no more particles are available (shown as "0 in free list"):

```
Router# show buffers
[text omitted]
Private particle pools:
Serial4/0 buffers, 512 bytes (total 192, permanent 192):
     0 in free list (0 min, 192 max allowed)
     192 hits, 0 fallbacks
     192 max cache size, 128 in cache
     10 buffer threshold, 0 threshold transitions
Serial4/1 buffers, 512 bytes (total 192, permanent 192):
     0 in free list (0 min, 192 max allowed)
     192 hits, 0 fallbacks
     192 max cache size, 128 in cache
     10 buffer threshold, 0 threshold transitions
Serial4/2 buffers, 512 bytes (total 192, permanent 192):
     0 in free list (0 min, 192 max allowed)
```

```
     192 hits, 0 fallbacks
     192 max cache size, 128 in cache
     10 buffer threshold, 0 threshold transitions
Serial4/3 buffers, 512 bytes (total 192, permanent 192):
     0 in free list (0 min, 192 max allowed)
     192 hits, 0 fallbacks
     192 max cache size, 128 in cache
     10 buffer threshold, 0 threshold transitions
ATM5/0 buffers, 512 bytes (total 1200, permanent 1200):
    0 in free list (0 min, 1200 max allowed)
    1200 hits, 1 misses
```

Step 3 To verify the percentage of the particle pool that is configured for possible allocation by the receive ring for a particular PVC, use the **show atm pvc** command. The following example shows that the receive ring limit is 25 percent for PVC 1/100:

```
Router# show atm pvc 1/100
 ATM1/0.1: VCD: 14, VPI: 1, VCI: 100
 UBR, PeakRate: 149760
 AAL5-LLC/SNAP, etype:0x0, Flags: 0xC20, VCmode: 0x0
 OAM frequency: 0 second(s), OAM retry frequency: 1 second(s),
 OAM retry frequency: 1 second(s)
 OAM up retry count: 3, OAM down retry count: 5
 OAM Loopback status: OAM Disabled
 OAM VC state: Not Managed
 ILMI VC state: Not Managed
 Rx Limit: 25 percent
 InARP frequency: 15 minutes(s)
 Transmit priority 4
 InPkts: 0, OutPkts: 0, InBytes: 0, OutBytes: 0
 InPRoc: 0, OutPRoc: 0
 InFast: 0, OutFast: 0, InAS: 0, OutAS: 0
 InPktDrops: 0, OutPktDrops: 0
 CrcErrors: 0, SarTimeOuts: 0, OverSizedSDUs: 0,
 LengthViolation: 0, CPIErrors: 0
 Out CLP=1 Pkts: 0
 OAM cells received: 0
 F5 InEndloop: 0, F5 InSegloop: 0, F5 InAIS: 0, F5 InRDI: 0
 F4 InEndloop: 0, F4 InSegloop: 0, F4 InAIS: 0, F4 InRDI: 0
 OAM cells sent: 0
 F5 OutEndloop: 0, F5 OutSegloop: 0, F5 OutRDI: 0
 F4 OutEndloop: 0, F4 OutSegloop: 0, F4 OutRDI: 0
 OAM cell drops: 0
 Status: UP
```

Note In later releases of the Cisco IOS software, the **show atm pvc** command displays the receive ring limit in the "VC Rx Limit" field as a number of private interface particles. The receive limit output was modified from percentages to particles in some of the following Cisco IOS software releases: 12.2(4)T, 12.2(9)S, 12.2(4)B, 12.2(3), 12.1(9)E, and 12.1(10).

The following example displays **show** output using Cisco IOS Release 12.2(10):

```
Router# show atm pvc 1/101
ATM6/0: VCD: 2, VPI: 1, VCI: 101
UBR, PeakRate: 149760
AAL5-LLC/SNAP, etype:0x0, Flags: 0xC20, VCmode: 0x0
OAM frequency: 0 second(s), OAM retry frequency: 1 second(s), OAM retry
frequency: 1 second(s)
OAM up retry count: 3, OAM down retry count: 5
OAM Loopback status: OAM Disabled
OAM VC state: Not Managed
```

```
ILMI VC state: Not Managed
VC TxRingLimit: 40 particles
VC Rx Limit: 800 particles
[text omitted]
```

Note On the PA-A3 and PA-A6 ATM port adapters for the Cisco 7200 series router, the **show** output always displays the value of the receive ring limit whether it is set by default or it is manually configured. However, on the Cisco 7500 series router, you can only show the value of the receive ring limit when you have manually configured the **rx-limit** command.

Configuring the Transmit Ring Limit

This section provides guidleines for configuring and verifying the transmit ring limit. It includes the following topics:

Transmit Ring Limit Configuration Guidelines

It is important for you to understand that QoS policies for ATM traffic are applied in the Layer 3 queues prior to the receipt of packets on the transmit ring. These QoS policies can affect which packets arrive to the transmit queue soonest based on the service policies for the class. However, the transmit ring itself uses a FIFO-based queue. Therefore, you do not want to optimize flow at the Layer 3 level, only to introduce high latencies at the transmit ring.

The primary consideration for tuning the transmit ring is finding the appropriate size of the transmit ring that is small enough to avoid latency in the ring's FIFO queue, but large enough to avoid drops that have a significant impact on TCP-based flows.

In general, low values are recommended for voice VCs and higher values are recommended for data VCs. Low values reduce jitter and delay due to queueing, and high values accommodate bursts.

Consider the following general guidelines when planning to tune the transmit ring limit:

- Configure the **tx-ring-limit** command as a number of ring entries, which equates to a number of particles in the private interface pool.
- Configure higher values for high-speed VCs.
- Lower the size of the transmit ring when you want to achieve packet differentiation using Layer 3 service policies and to avoid latency on the hardware queue.
- Configure a low value for low-bandwidth VCs, such as VCs with an SCR of 128 Kbps.

Note Packets are queued to the transmit ring as soon as there is a free particle, even if the packet requires more than one particle to be stored.

Transmit Ring Guidelines for Voice VCs

For VCs carrying voice traffic, reduce the size of the transmit ring limit. Select a value based on the amount of serialization delay, expressed in seconds, that is introduced by the transmit ring. To determine the amount of delay, you can use the following formula:

[(P x 8) x D] / S

where

P = Packet size in bytes (Multiply by eight to convert to bits.)

D = Transmit ring depth

S = Speed of the VC in bps

Transmit Ring Guidelines for Data VCs

For VCs carrying data, use the following guidelines:

- Consider the packet size and configure the **tx-ring-limit** command to accommodate 4 packets. Be aware that 64 bytes are always reserved in the first particle for header rewrites. Therefore, as an example, a 1500-byte packet requires 4 particles (of size 512 bytes). Multiplying 4 particles x 4 packets yields 16 for the the **tx-ring-limit** value.
- Be sure that the transmit ring limit is large enough to support one MTU-sized packet or the number of cells equal to the maximum burst size (MBS) for a nrt-VBR PVC.
- Use Table 7-1 for suggested transmit ring limits by link speed, when other specific guidelines do not apply:

Table 7-1 Suggested Transmit Ring Limit Values by Link Speed

Link Speed	Transmit Ring Limit
Less than or equal to 128 Kbps	5
192 Kbps	6
256 Kbps	7
512 Kbps	14
768 Kbps	21

- Tune the size of the queue when you think that the VC is experiencing unnecessary delay. On any network interface, queueing forces a choice between latency and the amount of burst that the interface can sustain. Larger queue sizes sustain longer bursts, but increase delay.

Default Values for the Transmit Ring Limit

The PA-A3 and PA-A6 ATM port adapters assign a default transmit ring limit for every VC. The way that this default value is determined varies by the service category that is configured for the VC. Table 7-2 shows how the default values for the transmit ring are implemented.

Table 7-2 Default Values for the Transmit Ring Limit by ATM Service Category

Service Category	Default Value	Time of Enforcement
ABR	128	Always
CBR	Calculated using the following formula: (48 x PCR) / (particle_size x 5) The minimum default value is 40. • The PCR includes ATM overhead, and is translated to cells per second for this formula. • The particle_size is 580 bytes, reflecting the particle size of the transmit hardware buffer on the ATM port adapter.	Always
UBR	• PA-A3 and PA-A6 (T3/E3/OC-3)—40 • PA-A3 IMA (T1/E1)—128	When the total credit utilization exceeds 75 percent of the tx_threshold value shown in the **show controllers atm** command output[1]
nrt-VBR	Calculated using the following formula: (48 x SCR) / (particle_size x 5) The minimum default value is 40. • The SCR includes ATM overhead, and is translated to cells per second for this formula. • The particle_size is 580 bytes, reflecting the particle size of the transmit hardware buffer on the ATM port adapter.	Always
rt-VBR	Same as nrt-VBR calculation.	Always

1. The tx_threshold value is used as an upper boundary for the PA-A3 or PA-A6 ATM port adapter to use during processing of UBR VCs. The PA-A3 and PA-A6 ATM port adapters allow for larger bursts on UBR VCs by enforcing the transmit limit on such VCs only when the total packet buffer usage on the PA-A3 or PA-A6 reaches 75 percent of this preset threshold.

Verifying the Default Transmit Ring Limit

To verify the default number of particles that can be used by a particular PVC for transmit processing during setup of a VC, you can use the **debug atm events** command. The following steps show the default transmit ring limit value assigned to a nrt-VBR PVC as it is configured:

Step 1 From global configuration mode, enable the **debug atm events** command:

```
Router(config)# debug atm events
```

Step 2 Configure a nrt-VBR PVC on an ATM interface and enable logging to display the debug messages on the console as shown in the following example. The default transmit limit is shown in the "vc tx_limit" field as 137:

```
Router(config)# interface atm 4/0
Router(config-if)# pvc 1/100
Router(config-if-atm-vc)# vbr-nrt 4000 3500 94
Router(config-if-atm-vc)#
*Oct 14 17:56:06.886:  Reserved bw for 1/100 Available bw = 141500
Router(config-if-atm-vc)# exit
Router(config-if)# logging
*Oct 14 17:56:16.370: atmdx_setup_vc(ATM4/0): vc:6 vpi:1 vci:100 state:2 config_status:0
*Oct 14 17:56:16.370: atmdx_setup_cos(ATM4/0): vc:6 wred_name:- max_q:0
*Oct 14 17:56:16.370: atmdx_pas_vc_setup(ATM4/0): vcd 6, atm hdr 0x00100640, mtu 4482
*Oct 14 17:56:16.370: VBR: pcr 9433, scr 8254, mbs 94
*Oct 14 17:56:16.370:  vc tx_limit=137, rx_limit=47
*Oct 14 17:56:16.374:  Created 64-bit VC count
```

Step 3 Based on an SCR of 3500 Kbps, the PA-A3 assigns a default tx_limit of 137. To see how this calculation is made, convert the SCR of 3500 Kbps to cells/sec.

- First change the SCR to a number of bytes/sec, (3,500,000 bits/sec) / 8 bits/byte = 437,500 bytes/sec.
- Then, divide by 53 bytes to determine the number of cells per second. (437,500 bytes/sec) / 53 bytes = 8254 cells/sec.

Step 4 Now, you can apply the formula for the default transmit ring limit of (48 x SCR) / (particle_size x 5). (48 x 8254) / (580 x 5) = 136.6, rounded to 137.

Transmit Ring Configuration Example

The following example specifies that PVC 1/121 can use 10 particles for data awaiting transmission:

Note The available range within the CLI for the transmit ring limit reflects the number of particles available in the transmit hardware buffer located on the ATM port adapter. This makes sense because the PVC might support multiple ingress interfaces. Therefore, the credit check on the number of private interface particles in use must not exceed the number of particles available in the hardware buffer on the ATM port adapter.

```
Router# configure terminal
Enter configuration commands, one per line.  End with CNTL/Z.
Router(config)# interface atm 5/0.2
Router(config-if)# pvc 1/121
Router(config-if-atm-vc)# tx-ring-limit ?
  <3-6000> Number (ring limit)
```

```
Router(config-if-atm-vc)# tx-ring-limit 10
Router(config-if-atm-vc)# end
```

Verifying the Transmit Ring Limit

Note On the PA-A3 and PA-A6 ATM port adapters for the Cisco 7200 series router, the **show** output always displays the value of the transmit ring limit whether it is set by default or it is manually configured. However, on the Cisco 7500 series router, you can only show the value of the transmit ring limit when you have manually configured the **tx-ring-limit** command.

To verify the number of particles that can be used by a particular PVC for transmit processing, you can use the **show atm vc** or the **show atm pvc** commands. The following **show atm vc** command example shows that the transmit ring limit is 10 particles for VC 1/121:

```
Router# show atm vc 5
ATM3/0.21: VCD: 5, VPI: 1, VCI: 121
UBR, PeakRate: 149760
AAL5-LLC/SNAP, etype:0x0, Flags: 0xC20, VCmode: 0x0
OAM frequency: 0 second(s)
VC TxRingLimit: 10 particles
VC Rx Limit: 120 particles
InARP frequency: 15 minutes(s)
Transmit priority 6
InPkts: 5, OutPkts: 379, InBytes: 540, OutBytes: 27380
InCells: 0, OutCells: 761
InPRoc: 5, OutPRoc: 379
InFast: 0, OutFast: 0, InAS: 0, OutAS: 0
InPktDrops: 0, OutPktDrops: 0/0/0 (holdq/outputq/total)
InCellDrops: 0, OutCellDrops: 0
InByteDrops: 0, OutByteDrops: 0
CrcErrors: 0, SarTimeOuts: 0, OverSizedSDUs: 0, LengthViolation: 0, CPIErrors: 0
Out CLP=1 Pkts: 0, Cells: 0
OAM cells received: 0
OAM cells sent: 0
Status: UP
```

The following **show atm pvc** command example for another PVC shows that a transmit ring limit of 40 particles:

```
Router# show atm pvc 1/101
ATM6/0: VCD: 2, VPI: 1, VCI: 101
UBR, PeakRate: 149760
AAL5-LLC/SNAP, etype:0x0, Flags: 0xC20, VCmode: 0x0
OAM frequency: 0 second(s), OAM retry frequency: 1 second(s), OAM retry
frequency: 1 second(s)
OAM up retry count: 3, OAM down retry count: 5
OAM Loopback status: OAM Disabled
OAM VC state: Not Managed
ILMI VC state: Not Managed
VC TxRingLimit: 40 particles
VC Rx Limit: 800 particles
[text omitted]
```

Monitoring Ring Limits and Resource Usage

It is important to understand the architecture involved in the processing of ATM traffic on the Cisco 7200 series router. Drops can occur due to a limitation of buffer resources either on board the ATM port adapter, or in the private interface pool on the NPE or NSE. Therefore, you should understand how to properly monitor the performance of your system's resources so that you can properly interpret where performance tuning might be appropriate.

This section describes some of the **show** commands that you can use to monitor the status of your input and output buffer resources located on the ATM port adapter hardware, and in the private interface pools on the the NPE or NSE. It includes the following topics:

Monitoring Hardware Buffers

The PA-A3 and PA-A6 ATM port adapters use memory on board the port adapter to store data for SAR processing. These ATM port adapters have a separate buffer for receive path processing, and another buffer for transmit path processing. The particle sizes vary in these two hardware buffers. For more information about the PA-A3 and PA-A6 ATM port adapter architecture, see the "Receive Buffer and Transmit Buffer Located on the PA-A3 and PA-A6 ATM Port Adapters" section on page 2-14.

The topics in this section describe how to determine whether you are experiencing a shortage of memory in the hardware buffers on the PA-A3 and PA-A6 ATM port adapters.

Monitoring the Status of Input Buffers Located on the PA-A3 and PA-A6 ATM Port Adapters

To monitor the status of the receive hardware buffer on the ATM port adapter, run the **show controllers atm** command and observe the "rx_no_buffer" counter. The following example indicates that there is not a shortage of input buffers because no packets have been dropped due to the VC reaching its transmit ring quota (shown by "rx_no_buffer=0"):

```
Router# show controllers atm 3/0
   Interface ATM3/0 is up
   Hardware is ENHANCED ATM PA - DS3 (45Mbps)
   Lane client mac address is 0030.7b1e.9054
   Framer is PMC PM7345 S/UNI-PDH, SAR is LSI ATMIZER II
   Firmware rev: G119, Framer rev: 1, ATMIZER II rev: 3
     idb=0x61499630, ds=0x6149E9C0, vc=0x614BE940
     slot 3, unit 2, subunit 0, fci_type 0x005B, ticks 73495
     400 rx buffers: size=512, encap=64, trailer=28, magic=4
   Curr Stats:
     rx_cell_lost=0, rx_no_buffer=0, rx_crc_10=0
     rx_cell_len=0, rx_no_vcd=0, rx_cell_throttle=0, tx_aci_err=0
[text omitted]
```

Monitoring the Status of Output Buffers Located on the PA-A3 and PA-A6 ATM Port Adapter

To determine when a shortage of output hardware buffers is occurring, complete the following steps:

Step 1 Run the **show interface atm** command and observe the "no buffer" counter. When the PA-A3 or PA-A6 ATM port adapter runs out of hardware storage in the transmit buffer on board the port adapter, the no buffer counter increments in the **show interface atm** command, as shown in the following example:

```
Router# show interface atm 4/0
    ATM4/0 is up, line protocol is up
    Hardware is ENHANCED ATM PA
    MTU 4470 bytes, sub MTU 4470, BW 149760 Kbit, DLY 80 usec,
    reliability 255/255, txload 136/255, rxload 1/255
    Encapsulation ATM, loopback not set
    Encapsulation(s): AAL5
    4095 maximum active VCs, 5 current VCCs
    VC idle disconnect time: 300 seconds
    Signalling vc = 4, vpi = 0, vci = 5
    UNI Version = 3.0, Link Side = user
    4 carrier transitions
    Last input 00:02:30, output 00:00:00, output hang never
    Last clearing of "show interface" counters never
    Input queue: 0/75/0/0 (size/max/drops/flushes); Total output drops: 103197668
    Queueing strategy: Per VC Queueing
    30 second input rate 0 bits/sec, 0 packets/sec
    30 second output rate 80210000 bits/sec, 6650 packets/sec
    308 packets input, 9856 bytes, 4138 no buffer
    Received 0 broadcasts, 0 runts, 0 giants, 0 throttles
    0 input errors, 0 CRC, 0 frame, 0 overrun, 0 ignored, 0 abort
    338179038 packets output, 3163620726 bytes, 0 underruns
    0 output errors, 0 collisions, 0 interface resets
    0 output buffer failures, 0 output buffers swapped out
```

Step 2 To further verify that the transmit hardware buffer is full, use the **show controllers atm** command and observe the value of the BFD cache status area of the output. The BFD cache "size" field indicates the total number of buffers in the local port adapter memory. The current number of free particles is shown by the "read" field. The PA-A3 reserves 144 particles for system packets like Operation, Administration, and Maintenance (OAM) cells. When the "read" value reaches 144, the PA-A3 driver starts dropping packets until a sufficient number of local memory particles becomes available. The following example shows that the free local memory particles for the hardware transmit buffer is 143, and therefore there is no available local hardware storage for transmit processing:

```
Router# show controllers atm 5/0
[text omitted]
   BFD Cache status:
     base=0x62931AA0, size=6144, read=143
   Rx Cache status:
[text omitted]
```

Monitoring Ring Limits for the Private Interface Pool

The topics in this section describe how to determine whether you are experiencing a shortage of memory in the private interface pool for receive or transmit processing on a PA-A3 or PA-A6 ATM port adapter.

Determining a Shortage of Private Interface Particles for Receive Processing

To determine if packets are being dropped due to a shortage of private interface particles for receive processing, use the **show interface atm** command and observe the "ignored" field. The following example shows that particles are still available for receive processing on ATM interface 4/0 because no packets have been dropped (shown by the "0 ignored" field):

```
Router# show interface atm 4/0
    ATM4/0 is up, line protocol is up
    Hardware is ENHANCED ATM PA
    MTU 4470 bytes, sub MTU 4470, BW 149760 Kbit, DLY 80 usec,
    reliability 255/255, txload 136/255, rxload 1/255
    Encapsulation ATM, loopback not set
    Encapsulation(s): AAL5
    4095 maximum active VCs, 5 current VCCs
    VC idle disconnect time: 300 seconds
    Signalling vc = 4, vpi = 0, vci = 5
    UNI Version = 3.0, Link Side = user
    4 carrier transitions
    Last input 00:02:30, output 00:00:00, output hang never
    Last clearing of "show interface" counters never
    Input queue: 0/75/0/0 (size/max/drops/flushes); Total output drops: 103197668
    Queueing strategy: Per VC Queueing
    30 second input rate 0 bits/sec, 0 packets/sec
    30 second output rate 80210000 bits/sec, 6650 packets/sec
    308 packets input, 9856 bytes, 4138 no buffer
    Received 0 broadcasts, 0 runts, 0 giants, 0 throttles
    0 input errors, 0 CRC, 0 frame, 0 overrun, 0 ignored, 0 abort
    338179038 packets output, 3163620726 bytes, 0 underruns
    0 output errors, 0 collisions, 0 interface resets
    0 output buffer failures, 0 output buffers swapped out
```

For more information about verifying the private interface particles, see the "Verifying the Receive Ring Limit and Particle Buffers" section on page 7-5.

Determining When the Transmit Ring Limit is Reached on a VC

To determine when a VC has reached its transmit ring limit quota, run the **show atm vc** command and observe the "OutPktDrops" counter. The following example indicates that the PVC 2/2 still has not reached its transmit quota because no packets have been dropped (shown by "OutPktDrops: 0"):

```
Router# show atm vc
VC 3 doesn't exist on interface ATM3/0
ATM5/0.2: VCD: 3, VPI: 2, VCI: 2
VBR-NRT, PeakRate: 30000, Average Rate: 20000, Burst Cells: 94
AAL5-LLC/SNAP, etype:0x0, Flags: 0x20, VCmode: 0x0
OAM frequency: 0 second(s)
PA TxRingLimit: 10
InARP frequency: 15 minutes(s)
Transmit priority 2
InPkts: 0, OutPkts: 0, InBytes: 0, OutBytes: 0
InPRoc: 0, OutPRoc: 0
InFast: 0, OutFast: 0, InAS: 0, OutAS: 0
InPktDrops: 0, OutPktDrops: 0
CrcErrors: 0, SarTimeOuts: 0, OverSizedSDUs: 0
OAM cells received: 0
OAM cells sent: 0
Status: UP
```

Note The **show controllers atm** command provides some transmit counter fields, such as "max_tx_count," "tx_count," and "tx_threshold." However, these output fields display the amount of transmit credits for the entire interface, not on an individual VC. For example, the "max_tx_count" field shows the maximum number of transmit particles held by the PA-A3 or PA-A6 ATM microcode. The "tx_count" field shows the total number of transmit particles currently being held by the port adapter microcode for all VCs. The "tx_threshold" field shows the preset limit used by the PA-A3 and PA-A6 ATM port adapters for enforcement of transmit limits on UBR PVCs.

Related Documentation

The following table provides information about additional resources that you can read to learn more about some of the topics discussed in this chapter:

For more information about :	Refer to the following publications:
MTUs on ATM port adapters	Understanding Maximum Transmission Unit (MTU) on ATM Interfaces (TAC Tech Note)
Troubleshooting input and output errors and interpreting **show** commands	• Troubleshooting Input and Output Errors on PA-A3 ATM Port Adapters (TAC Tech Note) • When Does the no buffer Error Counter Increment on the PA-A3?(TAC Tech Note) • Troubleshooting "Ignored" Errors on an ATM Port Adapter (TAC Tech Note)

Next Steps

This chapter describes how to optimize and verify the receive ring and transmit ring limits on the PA-A3 and PA-A6 ATM port adapters. If you want to know more about the memory architecture and the flow of ATM traffic processing using the receive rings, transmit rings, and the hardware buffers located on the PA-A3 and PA-A6 ATM port adapters, read Chapter 2, "Cisco 7200 Series Architecture and Design for ATM Traffic Management."

Chapter 8, "ATM Traffic Management Case Studies and Configuration Examples," provides case studies and configuration examples of some real-world implementations of ATM in enterprise networks, including tuning of transmit ring limits.